

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1-31. (Canceled).

32. (Withdrawn) A method of high frequency operation in an integrated circuit, said method comprising:

accessing charge stored in a capacitor comprising a plurality of deep n well regions formed in an epitaxy region of said integrated circuit; and

coupling said charge to a transistor device of said integrated circuit enabling switching at said high frequency.

33. (Withdrawn) The method of Claim 32 wherein said capacitor further comprises bulk p + material.

34. (Withdrawn) The method of Claim 32 wherein said capacitor further comprises a p well.

35. (Withdrawn) The method of Claim 32 wherein said coupling is parasitic.
36. (Withdrawn) The method of Claim 32 wherein said plurality of deep n well regions comprise substantially parallel stripes.
37. (Withdrawn) The method of Claim 32 wherein said plurality of deep n well regions comprise a grid.
38. (Withdrawn) The method of Claim 32 wherein said plurality of deep n well regions comprise more than one layer of deep n well.
39. (Previously Presented) An integrated circuit comprising:
- a plurality of transistors having a principal operating voltage;
 - a deep n well capacitor structure comprising;
 - a deep n well comprising n-type material coupled to said principal operating voltage; and

p-type material disposed proximate said deep n well and coupled to a ground reference.

40. (Previously Presented) The integrated circuit of Claim 39 wherein said deep n well is substantially surrounded by said p-type material.

41. (Previously Presented) The integrated circuit of Claim 39 comprising a plurality of said deep n wells.

42. (Previously Presented) The integrated circuit of Claim 39 wherein said deep n well is parasitically coupled to said principal operating voltage.

43. (Previously Presented) The integrated circuit of Claim 39 wherein said p-type material comprises epitaxy.

44. (Previously Presented) The integrated circuit of Claim 39 wherein said p-type material comprises bulk p material.

45. (Previously Presented) The integrated circuit of Claim 39 wherein said p-type material comprises a p well.

46. (Previously Presented) The integrated circuit of Claim 45 wherein said p well is at substantially a same depth as said deep n well.

47. (Withdrawn) An integrated circuit comprising:

a first deep n well at a first depth to supply on-chip decoupling capacitance; and

a second deep n well at a second depth to supply on-chip decoupling capacitance.

48. (Withdrawn) The integrated circuit of Claim 47 wherein said first and said second deep n wells are coupled together.

49. (Withdrawn) The integrated circuit of Claim 47 further comprising a plurality of transistors having a principal operating voltage and wherein said first and said second deep n wells are coupled to said principal operating voltage of said plurality of transistors of said integrated circuit.

50. (Withdrawn) The integrated circuit of Claim 47 wherein said first and said second deep n wells are coupled to a ground reference for said integrated circuit.

51. (Withdrawn) The integrated circuit of Claim 47 wherein said first and said second deep n wells are substantially surrounded by p type material.

52. (Withdrawn) The integrated circuit of Claim 47 wherein said first and said second deep n wells are formed with the same process mask.

53. (Withdrawn) The integrated circuit of Claim 51 wherein said first and said second deep n wells substantially surrounded by said p type material to form a power supply decoupling capacitor.

54. (Withdrawn) The integrated circuit of Claim 47 comprising a p well at substantially said first depth.

55. (Withdrawn) An integrated circuit as described in Claim 47 further comprising a deep p well disposed between said first and said second deep n wells.

56. (Withdrawn) A deep n well capacitor comprising a deep n well region of an integrated circuit, said deep n well coupled to Vdd and ground and has a surface area selected to provide a specified amount of capacitance.

57. (Withdrawn) The deep n well capacitor of Claim 56 further comprising a plurality of deep n well regions coupled together.

58. (Withdrawn) The deep n well capacitor of Claim 57 wherein said plurality of deep n well regions are substantially parallel.

59. (Withdrawn) The deep n well capacitor of Claim 57 wherein said plurality of deep n well regions comprise deep n well regions at different depths of said integrated circuit.

60. (Withdrawn) The deep n well capacitor of Claim 57 comprising a plurality of p well regions at substantially the same depth as said plurality of deep n well regions and wherein said plurality of p well regions are disposed between said plurality of deep n well regions.

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61. (Withdrawn) The deep n well capacitor of Claim 56 wherein said deep n well region is substantially surrounded by p type material.

62. (Withdrawn) The deep n well capacitor of Claim 56 wherein said deep n well region is parasitically coupled to said Vdd.